In re Patent Application of
DE LAURENTIIS ET AL.
Serial No. **Not Yet Assigned**
Filed: **Herewith**
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In the Claims:

Claims 1-8 (Cancelled).

9. (New) A method for amplifying with pre-emphasis a digital signal representative of data to be transmitted by a line driver over an output line, the method comprising:

varying a gain of the line driver between an upper value to coincide with switching of the digital signal and a lower value in absence of the digital signal switching, the varying comprising

amplifying the digital signal with a first gain for generating an amplified digital signal,

delaying the digital signal with a predetermined delay for generating a delayed digital signal,

amplifying the delayed digital signal with a second gain for generating a delayed and amplified digital signal, and

outputting over the output line an ouput signal corresponding to a difference between the amplified digital signal and the delayed and amplified digital signal.

10. (New) A method according to Claim 9, wherein the predetermined delay is equal to duration of a bit pulse of the digital signal.

11. (New) A method according to Claim 9, wherein the predetermined delay is less than duration of a bit pulse of the digital signal.

12. (New) A method according to Claim 9, wherein the line driver comprises an input circuit having a first input signal path for receiving the digital signal and a second input signal path for receiving an inverted digital signal.

13. (New) A method according to Claim 12, wherein the first input signal path comprises:

a first D-type flip-flop being clocked by an externally generated timing signal, and receiving as input the digital signal and outputting the digital signal; and

a delay circuit having the predetermined delay, and receiving as input the digital signal and outputting the delayed digital signal; and

wherein said second input signal path comprises:

a first D-type flip-flop being clocked by the externally generated timing signal, and receiving as input the inverted digital signal and outputting the inverted digital signal; and

a delay circuit having the predetermined delay, and receiving as input the inverted digital signal and outputting a delayed inverted digital signal.

14. (New) A method according to Claim 13, wherein the line driver further comprises first and second low voltage differential signal (LVDS) cells, with output nodes thereof being connected in common for providing the output signal as a differential pair of output signals.

15. (New) A method according to Claim 14, wherein the first LVDS cell is driven by the digital signal and by the

inverted digital signal; and wherein the second LVDS cell is driven by the delayed digital signal and by the delayed inverted digital signal.

16. (New) A method according to Claim 14, wherein respective bias currents for the first and second LVDS cells is equal to a ratio between the first and second gains.

17. (New) A method according to Claim 13, wherein the externally generated timing signal comprises a clock signal that generates the digital signal.

18. (New) A method according to Claim 13, wherein a frequency of the externally generated timing signal is a multiple of a frequency of a clock signal that generates the digital signal.

19. (New) An amplification circuit for amplifying a digital signal representative of data to be transmitted over an output line, the amplification circuit comprising:

a driver with pre-emphasis having a gain that varies between an upper to coincide with switching of the digital signal and a lower value in absence of the digital signal switching, said driver comprising

an input circuit for receiving the digital signal, and for providing a delayed digital signal, and

an output circuit for receiving the digital signal amplified with a first gain and for receiving the delayed digital signal amplified with a second gain, said output circuit for providing an

output signal over the output line by determining a difference between the amplified digital signal and the delayed and amplified digital signal.

20. (New) An amplification circuit according to Claim 19, wherein said input circuit comprises a first input signal path for the digital signal and a second input signal path for an inverted digital signal.

21. (New) An amplification circuit according to Claim 20, wherein said first input signal path comprises:

a first D-type flip-flop being clocked by an externally generated timing signal, and receiving as input the digital signal and outputting the digital signal; and

a delay circuit having a predetermined delay, and receiving as input the digital signal and outputting a delayed digital signal; and

wherein said second input signal path comprises:

a first D-type flip-flop being clocked by the externally generated timing signal, and receiving as input the inverted digital signal and outputting the inverted digital signal; and

a delay circuit having the predetermined delay, and receiving as input the inverted digital signal and outputting a delayed inverted digital signal.

22. (New) An amplification circuit according to Claim 21, wherein said driver comprises first and second low voltage differential signal (LVDS) cells, with output nodes thereof being connected in common for providing the output signal as a differential pair of output signals.

23. (New) An amplification circuit according to Claim 22, wherein said first LVDS cell is driven by the digital signal and by the inverted digital signal; and wherein said second LVDS cell is driven by the delayed digital signal and by the delayed inverted digital signal.

24. (New) An amplification circuit according to Claim 23, wherein respective bias currents for said first and second LVDS cells is equal to a ratio between the first and second gains.

25. (New) An amplification circuit according to Claim 21, wherein said delay circuit in each input signal path comprises a second D-type flip-flop connected in cascade to said first D-type flip-flop.

26. (New) An amplification circuit according to Claim 21, wherein the externally generated timing signal comprises a clock signal that generates the digital signal.

27. (New) An amplification circuit according to Claim 21, wherein a frequency of the externally generated timing signal is a multiple of a frequency of a clock signal that generates the digital signal.

28. (New) An amplification circuit for amplifying a digital signal representative of data to be transmitted over an output line, the amplification circuit comprising:

a driver with pre-emphasis having a gain that varies between an upper value to coincide with switching of the

digital signal and a lower value in absence of the digital signal switching, said driver comprising

a first low voltage differential signal (LVDS) cell being driven by the digital signal and by an inverted digital signal, and

a second low voltage differential signal (LVDS) cell being driven by a delayed digital signal and by a delayed inverted digital signal,

said first and second LVDS cells being connected together so that output nodes thereof are connected in common for providing an output signal over the output line by determining a difference between an amplified digital signal and a delayed and amplified digital signal.

29. (New) An amplification circuit according to Claim 28, wherein the amplified digital signal has been amplified with a first gain, and wherein the delayed and amplified digital signal has been amplified with a second gain.

30. (New) An amplification circuit according to Claim 28, wherein the output nodes are connected together so that the output signal comprises a differential pair of output signals.

31. (New) An amplification circuit according to Claim 28, wherein said driver comprises an input circuit for receiving the digital signal, and for providing the delayed digital signal.

32. (New) An amplification circuit according to Claim 31, wherein said input circuit comprises a first input signal path for the digital signal and a second input signal path for an inverted digital signal.

33. (New) An amplification circuit according to Claim 32, wherein said first input signal path comprises:

a first D-type flip-flop being clocked by an externally generated timing signal, and receiving as input the digital signal and outputting the digital signal; and

a delay circuit having a predetermined delay, and receiving as input the digital signal and outputting the delayed digital signal; and

wherein said second input signal path comprises:

a first D-type flip-flop being clocked by the externally generated timing signal, and receiving as input the inverted digital signal and outputting the inverted digital signal; and

a delay circuit having the predetermined delay, and receiving as input the inverted digital signal and outputting the delayed inverted digital signal.

34. (New) An amplification circuit according to Claim 29, wherein respective bias currents for said first and second LVDS cells is equal to a ratio between the first and second gains.

35. (New) An amplification circuit according to Claim 33, wherein said delay circuit in each input signal path comprises a second D-type flip-flop connected in cascade to said first D-type flip-flop.

36. (New) An amplification circuit according to Claim 33, wherein the externally generated timing signal comprises a clock signal that generates the digital signal.

37. (New) An amplification circuit according to Claim 33, wherein a frequency of the externally generated timing signal is a multiple of a frequency of a clock signal that generates the digital signal.